WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising a cell array including a plurality of memory cells,

each of said memory cells including:

first and second switch transistors connected in series between a bit line for normal access and a bit line for refresh; and

a capacitor for data storage connected to a connection node at which the first and second switch transistors are tied;

the first and second switch transistors having control terminals connected to a word line for normal access and a word line for refreshing respectively;

said semiconductor memory device, being configured as a late-write configuration, in which a write to a memory cell selected by a write address supplied to an address terminal of said semiconductor memory device from an outside of said semiconductor memory device is performed with a delay of at least one write cycle from input of the write address, further comprising:

a sense amplifier for refreshing, connected to the bit line for refreshing:

a determination unit for comparing a refresh address with a row address of a write address externally supplied to the address terminal at least one write cycle before to determine whether the refresh address matches the row address or not to output a determination result; and

a control unit for performing control so that

when a mismatch between the refresh address and the row address

of the write address is detected by the determination circuit, a write operation and a refresh operation are performed concurrently in an identical cycle, in which the write operation is performed by activating the word line for normal access selected by the write address, turning on the first switch transistor in the memory cell connected to said word line for normal access, and writing data to the capacitor through the bit line for normal access, while the refresh operation is performed by activating the word line for refreshing selected by the refresh address, turning on the second switch transistor in the memory cell connected to said word line for refreshing, and reading a cell data and restoring said cell data through the bit line for refreshing by the sense amplifier for refreshing connected to the bit line for refreshing, and

when a match between the refresh address and the row address of the write address is detected by the determination circuit, the refresh operation is inhibited while the write operation is performed.

2. The semiconductor memory device according to claim 1, wherein said determination circuit compares the refresh address with the row address of the write address to detect whether the refresh address matches the row address of the write address or not before a cycle for performing the write operation on said cell array is started.

3. The semiconductor memory device according to claim 1, comprising:

a write address holding circuit for holding the write address externally supplied and for delaying the write address by a predetermined number of write cycles corresponding to the late-write

configuration to output the delayed write address;

a selection circuit, receiving a control signal for commanding a read /write operation as a selection control signal and receiving the externally input address and the address output from said write address holding circuit, for selecting the externally input address when the control signal indicates a read operation and for selecting the address output from said write address holding circuit when the control signal indicates a write to output the selected address, the address output from said selection circuit being supplied to an X decoder for selecting the word line for normal access; and

a match detection circuit for comparing the refresh address with the row address of the write address held in said write address holding circuit at a time point before output of the write address delayed by the predetermined number of write cycles is performed by the write address holding circuit to detect whether the refresh address matches the row address of the write address or not; wherein a judgement whether the row address of the write address matches the refresh address or not being performed before a cycle of performing the write operation on said memory cell on said cell array selected by the write address is started.

4. The semiconductor memory device according to claim 1, further comprising:

a write address holding circuit for holding the externally input write address and delaying the externally input write address by a predetermined number of write cycles corresponding to the late-write configuration to output the delayed write address;

a selection circuit, receiving a control signal for commanding a read /write operation as a selection control signal and receiving the externally input address and the address output from said write address holding circuit, for selecting the externally input address when the control signal indicates a read operation and for selecting the address output from said write address holding circuit when the control signal indicates a write operation to output the selected address, the address output from said selection circuit being supplied to an X decoder for selecting the word line for normal access; and

a match detection circuit for comparing the row address output from said selection circuit with the refresh address to detect whether the row address matches the refresh address or not.

5. The semiconductor memory device according to claim 1, further comprising:

a write address holding circuit for holding the externally input write address and delaying the externally input write address by a predetermined number of write cycles corresponding to the late-write configuration to output the delayed write address;

a first selection circuit, receiving a control signal for commanding a read/write operation as a selection control signal and receiving the externally input address and the address output from said write address holding circuit, for selecting the externally input address when the control signal indicates a read operation and for selecting the address output from said write address holding circuit when the control signal indicates a write operation to output the selected address, the

address output from said first selection circuit being supplied to an X decoder for selecting the word line for normal access;

a first match detection circuit for comparing the externally input row address with the refresh address to detect whether the row address matches the refresh address or not;

a second match detection circuit for comparing the refresh address with the row address of the write address held in said write address holding circuit at a time point before output of the write address delayed by the predetermined number of write cycles is performed to detect whether the refresh address matches the row address or not; and

a second selection circuit, receiving the control signal for commanding a read/write operation as a selection control signal and receiving output signals of said first and second match detection circuits, for selecting an output signal of said first match detection circuit when the control signal indicates the read operation and for selecting an output signal of said second match detection circuit when the control signal indicates write operation, to output the selected signal, the signal output from said second selection circuit being used as the determination result of said determination unit.

6. The semiconductor memory device according to claim 1, further comprising:

a control circuit, receiving the determination result output from said determination unit, for performing control so that

when there is at least one mismatching bit between the row address of the write address and the refresh address, a refresh control

signal for controlling the refresh operation is activated, and the refresh operation using the word line for refreshing, selected by the refresh address is performed concurrently with the write operation on said memory cell selected by the write address during the same cycle, and

when the row address of the write address and the refresh address match in all bit positions, the refresh control signal is deactivated to disable the refresh operation, and only the write operation on said memory cell selected by the write address is performed.

7. The semiconductor memory device according to claim 3, further comprising:

at least one third match detection circuit for comparing the externally input address with the write address, which is held in said write address circuit and which is at a stage before output from said write address holding circuit is performed, to detect whether the externally input address matches the write address or not; and

a control circuit for performing control so that write data associated with the write address, held in a data holding circuit during a period corresponding to the late-write configuration is output to a data output terminal as read data, when the write address matches an externally input read address.

8. The semiconductor memory device according to claim 1, wherein said semiconductor memory device includes:

a timer for generating a trigger signal for specifying a refresh cycle; and

a refresh address generation circuit for generating the refresh

address based on the trigger signal from said timer, on a same chip; and wherein

said semiconductor memory device is interface compatible with a static random access memory of a clock synchronous type.

9. The semiconductor memory device according to claim 1, comprising:

a first X decoder for decoding the row address of an input address externally supplied to the semiconductor memory device;

a second X decoder for decoding the refresh address, wherein the word line for normal access is connected to the first X decoder;

a first sense amplifier for normal access; and

a second sense amplifier constituting said sense amplifier for refreshing;

wherein

the word line for normal access is connected to the first X decoder;

the word line for refreshing is connected to the second X decoder;

said first and second X decoders are disposed to be opposite to each other with said cell array interposed therebetween;

the bit line for normal access is connected to the first sense amplifier;

the bit line for refreshing is connected to the second sense amplifier; and

said first and second sense amplifiers are disposed to be opposite to each other with respect to said cell array interposed therebetween.

10. A semiconductor memory device comprising:

a cell array having a plurality of memory cells;

a first X decoder for decoding a row address of an input address externally supplied to said semiconductor memory device;

a second X decoder for decoding a refresh address;

a first sense amplifier for normal access;

a second sense amplifier for refreshing;

a timer for generating a trigger signal for specifying a refresh cycle; and

a refresh address generation circuit, receiving the trigger signal output from said timer, for generating the refresh address based on the trigger signal;

wherein

each of said memory cells includes:

first and second switch transistors connected in series between a first bit line and a second bit line adjacent to each other; and

a capacitor for data storage connected to a connection node at which the first and second switch transistors are tied;

the first switch transistor having a control terminal connected to a first word line to be controlled on/off;

the second switch transistor having a control terminal connected to a second word line adjacent to the first word line to be controlled on/off;

and wherein

the first word line is connected to the first X decoder;

the second word line is connected to the second X decoder; said first and second X decoders being disposed to be opposite to each other with said cell array interposed therebetween;

the first bit line is connected to the first sense amplifier; and

the second bit line is connected to the second sense amplifier; said first and second amplifiers being disposed to be opposite to each other with said cell array interposed therebetween;

said semiconductor memory device further comprising:

a match detection circuit for comparing the refresh address from said refresh address generation circuit with the row address of the externally supplied write address delayed by a period corresponding to a predetermined number of write cycles to detect whether the refresh address matches the row address or not; and

a control unit for performing control so that

when a mismatch between the refresh address and the row address of the write address is detected by the match detection circuit, a write operation and a refresh operation are concurrently performed in an identical cycle, in which the write operation is performed by activating the first word line selected as a result of decoding the row address of the write address by said first X decoder, turning on the first switch transistor for the memory cell connected to the first word line, and writing data to said memory cell selected by the write address, while the refresh operation is performed by activating the second word line selected as a result of decoding the refresh address by said second X decoder and using said second sense amplifier on the memory cell

connected to the second word line, and

when the match between the refresh address and the row address of the write address is detected by the match detection circuit, the refresh operation is inhibited, the first word line selected by decoding by said first X decoder is activated, and then the write operation on said memory cell selected by the write address is performed.

11. The semiconductor memory device according to claim 10, further comprising:

an input buffer for receiving a row address of an input address externally supplied to said semiconductor memory device;

a first latch circuit for sampling an output signal of the input buffer using an internal clock signal as a sampling clock;

a second latch circuit for sampling the refresh address output from said refresh address generation circuit using the internal clock signal as a sampling clock;

a write address holding circuit including a plurality of latch circuits connected in cascade connection, each latching a signal at an input terminal thereof to output a sampled signal from an output terminal thereof using a clock signal for write control activated during a write cycle as a sampling clock,

a first stage of said latch circuits receiving an output signal of said first latch circuit at the input terminal thereof and a last stage of said latch circuits delaying the output signal of said first latch circuit by the predetermined number of write cycles to output the delayed signal from an output terminal thereof;

a selection circuit, receiving a control signal for commanding a read/write operation as a selection control signal and receiving the output signal of said first latch circuit and an output signal of said write address holding circuit, for selecting the output signal of said first latch circuit when the control signal indicates a read operation and selecting the output signal of said write address holding circuit when the control signal indicates a write operation to output the selected signal; and

a match detection circuit for comparing the output signal of said selection circuit with an output signal of said second latch circuit to detect whether the output signal of said selection circuit matches the output signal of said second latch circuit or not.

12. The semiconductor memory device according to claim 10, further comprising:

an input buffer for receiving a row address of an input address externally supplied to said semiconductor memory device;

a first latch circuit for sampling an output signal of the input buffer with an internal clock signal;

a second latch circuit for sampling the refresh address output from said refresh address generation circuit with the internal clock signal;

a write address holding circuit including a plurality of latch circuits connected in cascade connection, each sampling a signal at an input terminal thereof to output a sampled signal from an output terminal thereof with a clock signal for write control activated during a write cycle, a first stage of said latch circuits receiving an output signal

of said first latch circuit at the input terminal thereof and a last stage of said latch circuits delaying the output signal of said first latch circuit by the predetermined number of write cycles to output the delayed signal from the output terminal thereof;

a selection circuit, receiving the output signal of said first latch circuit and an output signal of said write address holding circuit, for selecting the output signal of said first latch circuit in case of a read operation and for selecting the output signal of said write address holding circuit in case of a write operation, according to a control signal for commanding a read/write operation to output the selected signal; and

a match detection circuit for comparing an output signal of said latch circuit at a stage preceding said last stage of said latch circuits in said write address holding circuit with an output signal of said second latch circuit to detect whether the output signal of said latch circuit matches the output signal of said second latch circuit or not.

13. The semiconductor memory device according to claim 10, further comprising:

an input buffer for receiving a row address of an input address externally supplied to said semiconductor memory device;

a first latch circuit for sampling an output signal of the input buffer with an internal clock signal;

a write address holding circuit including a plurality of latch circuits connected in cascade connection, each sampling a signal at an input terminal thereof to output a sampled signal from an output terminal thereof with a clock signal for write control activated during a

write cycle, a first stage of said latch circuits receiving an output signal of said first latch circuit at the input terminal thereof and a last stage of said latch circuits delaying the output signal of said first latch circuit by the predetermined number of write cycles to output the delayed signal from the output terminal thereof;

a first selection circuit, receiving a control signal for commanding a read/write operation as a selection control signal and receiving the output signal of said first latch circuit and an output signal of said write address holding circuit, for selecting the output signal of said first latch circuit when the control signal indicates a read operation and for selecting the output signal of said write address holding circuit when the control signal indicates a write operation to output the selected signal;

a first match detection circuit for comparing the externally input row address with the refresh address output from said refresh address generation circuit to detect whether the externally input row address matches the refresh address or not;

a second match detection circuit for comparing an output signal of a stage of said latch circuits preceding said last stage of said latch circuits in said write address holding circuit with the refresh address to detect whether the output signal of said stage matches the refresh address or not; and

a second selection circuit, receiving the control signal for commanding a read/write operation as a selection control signal and receiving output signals of said first and second match detection circuits,

for selecting an output signal of said first match detection circuit when the control signal indicates the read operation and for selecting an output signal of said second match detection circuit when the control signal indicates the write operation to output the selected signal.

14. The semiconductor memory device according to claim 11, wherein said write address holding circuit comprises pairs of latch circuits connected in cascade connection, each of said pairs of said latch circuits sampling data at falling or rising edge of the clock signal for write control, respectively, a number of said pairs being equivalent to the predetermined number of write cycles.

15. The semiconductor memory device according to claim 11, further comprising:

a data holding circuit for holding write data;

at least one match detection circuit for comparing the write address output from a stage of latch circuits preceding a last stage in said write address holding circuit with the externally input address to detect whether the write address matches the externally input address or not; and

a control circuit for performing control so that when the write address matches an externally input read address, write data associated with the write address and held at the data holding circuit during a period specified for a late write is output to a data output terminal as read data.

16. The semiconductor memory device according to claim 11, wherein a chip enable signal is employed for the internal clock signal and a write

enable signal is employed for the clock signal for write control.

17. The semiconductor memory device according to claim 16, wherein said write address holding circuit delays the externally input address by one write cycle.

18. The semiconductor memory device according to claim 10, wherein the semiconductor memory device is interface compatible with a clock synchronous type static random access memory.

19. A semiconductor memory device which has an interface compatible with that of a static random access memory compliant with a late-write specification, said semiconductor memory device comprising:

a cell array including a plurality of two-port DRAM cells;

a refresh address generation circuit;

a comparator for comparing a refresh address output from the refresh address generation circuit with a write address delayed by a period corresponding to a write access cycle defined in the late-write specification; and

a control unit for performing control so that a refresh operation is stopped when a comparison result by the comparator indicates that the refresh address matches the write address.

20. The semiconductor memory device according to claim 1, further comprising:

a sense amplifier for normal access, connected to the bit line for normal access; and

a control circuit for performing control so that when the normal access and the refresh are performed in an identical cycle, activation of

said sense amplifier for refreshing and activation of said sense amplifier for normal access are simultaneously started.

21. The semiconductor memory device according to claim 10, further comprising:

a control circuit for performing control so that when activation of said first sense amplifier and activation of said second sense amplifier are performed during the same cycle, the activation of said first sense amplifier and the activation of said second sense amplifier are simultaneously started.

22. A semiconductor memory device comprising:

a memory cell array including a read/write address input port and a refresh address input port, a read/write access to a memory cell therein specified by an address input from said read/write address input port and a refresh on a memory cell therein specified by an address input from said refresh address input port in synchronization with the read/write access being simultaneously performed;

an address holding circuit and a data holding circuit for holding the address supplied to an address terminal thereof from an outside of said semiconductor memory device and data supplied to a data terminal thereof from the outside of said semiconductor memory device, respectively;

a first determination circuit for comparing a row address held in said address holding circuit and the refresh address supplied from said refresh address input port to detect whether the row address matches the refresh address or not;

a second determination circuit for comparing the address held in said address holding circuit with an externally input read address to detect whether the address held in said address holding circuit matches the externally input read address or not;

a first control circuit for performing control so that

when said first determination circuit detects a mismatch, a write operation for writing the data held in said data holding circuit to the memory cell specified by the address, held in said address holding circuit and supplied to said memory cell array from said read/write address input port and a refresh operation on the refresh address are simultaneously performed, in synchronization with the write operation, and

when said first determination circuit detects the match, the refresh operation is inhibited and the write operation is performed; and

a second control circuit for performing control so that

when said second determination circuit detects a mismatch, the address held in said address holding circuit is supplied to the memory cell array from said read/write address input port and data is read from the memory cell specified by the address to output from said data terminal; and

when said second determination circuit detects the match, the data is read from said data holding circuit instead of said memory cell array to output from said data terminal.

23. The semiconductor memory device according to claim 5, further comprising:

at least one third match detection circuit for comparing the externally input address with the write address, which is held in said write address circuit and which is at a stage before output from said write address holding circuit is performed, to detect whether the externally input address matches the write address or not; and

a control unit for performing control so that write data associated with the write address, held in a data holding circuit during a period corresponding to the late-write configuration is output to a data output terminal as read data, when the write address matches an externally input read address.

24. The semiconductor memory device according to claim 12, wherein said write address holding circuit comprises pairs of latch circuits connected in cascade connection, each of said pairs of said latch circuits sampling data at falling or rising edge of the clock signal for write control, respectively, a number of said pairs being equivalent to the predetermined number of write cycles.

25. The semiconductor memory device according to claim 13, wherein said write address holding circuit comprises pairs of latch circuits connected in cascade connection, each of said pairs of said latch circuits sampling data at falling or rising edge of the clock signal for write control, respectively, a number of said pairs being equivalent to the predetermined number of write cycles.

26. The semiconductor memory device according to claim 19, wherein the semiconductor memory device has an interface compatible with that of a static random access memory compliant with zero bus turnaround

specifications.

27. A method of controlling a semiconductor memory device, said semiconductor memory device comprising: a cell array including a plurality of memory cells, each of said memory cells comprising:

first and second switch transistors connected in series between a bit line for normal access and a bit line for refreshing; and

a capacitor for data storage, connected to a connection node at which the first and second switch transistors are tied; a word line for normal access and a word line for refreshing being connected to respective control terminals of the first and second switch transistors;

said semiconductor memory device having a late-write configuration in which a write to a memory cell selected by a write address supplied to an address terminal of said semiconductor memory device from an outside of said semiconductor memory device is performed, being delayed by at least one write cycle; said method comprising the steps of:

comparing a generated refresh address with the write address externally supplied to the address terminal at least one write cycle earlier to detect whether the refresh address matches the write address or not;

performing control so that

when a mismatch between the refresh address and the row address of the write address is detected, a write operation and a refresh operation are concurrently performed in an identical cycle, in which the write operation is performed by activating the word line for normal

access selected by the write address, turning on the first switch transistor for the memory cell connected to said word line for normal access, and writing data to the capacitor through the bit line for normal access, while the refresh operation is performed by activating the word line for refreshing selected by the refresh address, turning on the second switch transistor for the memory cell connected to said word line for refreshing, and reading cell data and restoring said cell data through the bit line for refreshing using a sense amplifier for refreshing connected to said bit line for refreshing; and

when a match between the refresh address and the row address of the write address is detected, the refresh operation is inhibited and the write operation is performed.

28. The method according to claim 27, further comprising the step of:

comparing the refresh address with the write address to detect whether the refresh address matches the write address or not before a cycle of performing the write operation on said cell array is started.

29. A method of controlling a semiconductor memory device comprising a cell array including a plurality of memory cells each requiring a refreshing to hold stored data, an address holding circuit for holding an address input to an address terminal thereof, and a data holding circuit for holding data input to a data terminal thereof, the address and the data supplied from an outside of said semiconductor memory device, said method comprising the steps of:

storing the externally input address and the data in said address holding circuit and said data holding circuit, respectively;

comparing a row address of the write address held in said address holding circuit with a refresh address to detect whether the row address matches the refresh address or not, and simultaneously performing a write operation for writing the data held in said data holding circuit to said cell array and a refresh operation on said cell array when a mismatch between the row address of the write address and the refresh address is detected, and inhibiting the refresh operation and performing the write operation when the match between the row address of the write address and the refresh address is detected; and

comparing the write address held in said address holding circuit with an externally input read address to detect whether the write address matches the externally input read address or not, reading data from said cell array for supply from said data terminal when a mismatch is detected, and reading the data held in said data holding circuit for supply from said data terminal when the match is detected.

30. The method of controlling a semiconductor memory device according to claim 29, further comprising the step of:

comparing the externally input read address with the refresh address to detect whether the externally input read address matches the refresh address or not,

performing control to execute simultaneously the refresh operation on said cell array selected by the refresh address and reading data from said cell array selected by the read address when a mismatch is detected; and

performing control to inhibit the refresh operation and to execute

reading data from said cell array selected by the read address when a match is detected.